REMARKS

The Examiner is thanked for the interview courteously granted to the undersigned, on October 6, 2003, in connection with the above-identified application. Prior to this interview, proposed amended claims 1 and 54 were provided to the Examiner, for discussion during this interview. At the interview, it was pointed out how claims 1 and 54 as submitted to the Examiner prior to the interview were fully supported by Applicants' original disclosure, including the description therein in connection with the chemically mechanically polished surface. Moreover, differences between the subject matter of these amended claims 1 and 54, on the one hand, and the teachings of the applied prior art, including the two U.S. patents respectively to Mehta, et al. and to Mehta, on the other, were discussed, and advantages according to the present invention due to these differences were discussed by the undersigned.

During the interview, the Examiner pointed to Mehta, et al. as having a shallow and deep trench, respectively, and contended that Mehta, et al. did not include a LOCOS (local oxidation of silicon) field oxide of the semiconductor substrate. No agreement was reached during the interview.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, the claims have been amended to recite that the trench portion, or trench region, is "thermally" oxidized, e.g., so as to form a curvature of the upper end portion of the trench; and to recite that the insulating film is removed by chemical mechanical polishing, thereby forming a "chemically mechanically" polished surface. The claims have been further amended to recite the performing of selective thermal oxidation of the semiconductor substrate after having

formed the chemically mechanically polished surface, so as to (selectively) oxidize only a portion of the substrate, at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, in order to increase curvature of the upper end portion or upper corners of the trench, substantially without oxidizing other portions of the semiconductor substrate lining the trench.

Note, for example, the description in connection with the fabrication process of an MOS transistor according to the third embodiment, described on pages 19-25 of Applicants' specification, particularly the description from page 20, line 3 to page 25, line 7, of Applicants' specification. Note also, in particular, the last full paragraph on page 23, and the paragraph bridging pages 23 and 24, of Applicants' specification; and the description in the paragraph bridging pages 24 and 25 of Applicants' specification, that the additional oxidation need not always be carried out before etch-back of the buried insulating film 9, and may be carried out after etch-back of the buried insulating film 9 in accordance with the products specification required for products in the same way as in the first embodiment. Note also, for example, Fig. 2G and the disclosure at page 13, lines 15-22 of Applicants' specification, that the buried insulating film 9 is then etched back by chemical-mechanical polishing (CMP) or dry etching.

During the aforementioned interview, when chemical-mechanical polishing in connection with the first embodiment on page 13 of Applicants' specification as pointed out to the Examiner, the Examiner noted that Fig. 2 has been restricted out. However, it is respectfully submitted that for purposes of the first paragraph of 35 USC §112, all of Applicants' disclosure must be considered as to the guidance it provides to one of ordinary skill in the art with respect to all embodiments. Noting the description of

etching back the buried insulating film by chemical-mechanical polishing or dry etching, on page 13, lines 15-22 of Applicants' specification, together with disclosure of etching back the buried insulating film 9 on page 23, lines 3-11 of Applicants' specification, it is respectfully submitted that Applicants' disclosure as a whole fairly and completely provides guidance to one of ordinary skill in the art that the etching back of the buried insulating film 9 as shown in Figs. 6H and I can be performed, inter alia, by chemical-mechanical polishing. Note also the disclosure in the paragraph bridging pages 24 and 25 of Applicant's specification, in connection with the third embodiment, and referring back to the first embodiment. Thus, it is respectfully submitted that even though the embodiment of Fig. 2 is not being considered on the merits in the above-identified application, the description in connection therewith in Applicants' specification cannot be ignored in connection with a determination of satisfying the description requirement under the first paragraph of 35 USC §112.

Applicants respectfully traverse the objection to the Amendment filed June 5, 2003, under 35 USC §132, the Examiner contending that this Amendment filed June 5, 2003 introduces new matter into the disclosure. Specifically, the Examiner contends that the new matter which is not supported by the original disclosure is performing oxidation of the semiconductor substrate "having said polished surface".

Applicants have amended their claims to recite that the additional or selective thermal oxidation of the semiconductor substrate is performed "after" having "formed" the "chemically mechanically" polished surface. Clearly, this step of performing selective thermal oxidation of the semiconductor substrate after having formed the chemically mechanically polished surface is supported by Applicants' original

disclosure, in view of the disclosure of the additional oxidation being carried out after etch-back of the buried insulating film "in the same way as in the first embodiment", set forth in the paragraph bridging pages 24 and 25 of Applicants' specification, together with a description of the buried insulating film being etched back by chemical-mechanical polishing on page 13, lines 15-22 of Applicants' specification (that is, in the first embodiment). Clearly, where the additional oxidation is performed after etching back by chemical-mechanical polishing, a chemically mechanically polished surface is formed and the selective or additional thermal oxidation is performed after having formed the chemically mechanically polished surface. Thus, clearly, the present claims are described sufficiently to satisfy in light of the description requirement of the first paragraph of 35 USC §112, such that the objection to the Amendment filed June 5, 2003 is clearly improper insofar as applicable to amended claims presently in the application.

The contention by the Examiner in Item 2 on page 2 of the Office Action mailed July 3, 2003, that, at best, pages 7, 13 and 14 of the originally filed specification disclose that the buried insulating film is etched back by chemical-mechanical polishing or dry etching, is noted. However, it is respectfully submitted that by performing chemical mechanical polishing, a chemically mechanically polished surface would be formed; and by performing the additional oxidation after the etching back (that is, after forming the chemically mechanically polished surface), the performance of the additional oxidation would occur after having formed the chemically mechanically polished surface. Thus, even in light of the interpretation by the Examiner of Applicants' original disclosure, it is respectfully submitted that the original disclosure

supports the presently amended claims, such that the claims as presently amended do not include new matter.

The requirement by the Examiner to cancel the new matter in reply to the Office Action mailed July 3, 2003, is noted. It is respectfully submitted that in light of present claim amendments, any issue concerning new matter is moot; while Applicants do not consider previous amendments in the Amendment filed June 5, 2003, to be new matter, as set forth in the foregoing clearly the presently amended claims do not include new matter, such that any issue concerning new matter has been avoided in the present application.

Applicants respectfully traverse the rejection of their claims under the first paragraph of 35 USC §112, as set forth in Item 3 on pages 2 and 3 of the Office Action mailed July 3, 2003, particularly insofar as this rejection is applicable to the claims as presently amended. Thus, the Examiner contends that the claim recitation "performing oxidation of said semiconductor substrate **having said polished surface**" is not supported in the application as filed. As is clear from the foregoing, Applicants have amended their claims to recite performing additional oxidation of the semiconductor substrate "after" having "formed" the "chemically mechanically" polished surface. As seen in the foregoing analysis in connection with the objection to the Amendment filed June 5, 2003, as introducing new matter, clearly the present claim language is supported by Applicants' disclosure. Accordingly, any question as to a written description of the presently amended claims, with respect to oxidation of the semiconductor substrate "having said polished surface", is moot; and it is respectfully

submitted that the present claim language is clearly supported by Applicants' original disclosure, as discussed previously.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed July 3, 2003, that is, the teachings of the U.S. patents to Mehta, et al., No. 5,646,063, to Mehta, No. 5,679,599, and to Otsu, No. 5,236,861, and Japanese Patent Document No. 1-107554 (referred to by the Examiner as "Yuzuriha"), under the provisions of 35 USC §103.

It is respectfully submitted that the references as applied by the Examiner would have neither taught nor would have suggested such a method for fabricating a semiconductor device or semiconductor substrate as in the present claims, including, after forming a trench or trench region, thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench, so as to form, e.g., a first curvature of the upper end portion of the trench; and after burying a buried insulating film into the trench and on an oxidation prevention film on a substrate having the trench formed therein, removing the insulating film by chemical mechanical polishing and thereafter performing selective or additional thermal oxidation of the substrate after having formed the chemically mechanically polished surface, so as to thermally oxidize only a portion of the substrate, at the upper end portion of the trench, and not substantially at other portions of the substrate lining the trench, so as to increase a curvature of the upper end portion of the trench substantially without oxidizing the other portions of the semiconductor substrate lining the trench. See claim 1. Note also

claims 2, 4, 5, 9, 10 and 15, having corresponding recitations. Note similar recitations in claims 41, 43, 45, 46 and 47.

Moreover, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such method of fabricating a semiconductor device, as in the present claims, including forming the trench; thermally oxidizing a trench portion formed in the substrate and burying a buried insulating film into the trench so thermally oxidized, the insulating film also being formed on the oxidation prevention film; after burying the buried insulating film, performing an additional thermal oxidation so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench, to increase the radius of curvature in the proximity of the upper end portion of the trench, and substantially without oxidizing other portions of the semiconductor substrate lining the trench; and after burying the buried insulating film, removing the insulating film on the oxidation prevention film. See claim 54.

In general, and as will be discussed further infra, it is respectfully submitted that the applied references do not disclose, nor would have suggested, and in fact would have taught away from, the method of fabricating a semiconductor device as in the present claims, including the thermal oxidation of the trench and then, after burying insulation material in the trench, additional thermal oxidation to selectively oxidize the semiconductor substrate at the upper end portion of the trench, to increase the radius of curvature at the upper end portion and substantially without oxidizing other portions of the substrate lining the trench.

Furthermore, it is respectfully submitted that these references would have neither taught nor would have suggested the presently claimed method, having

features as discussed previously, and moreover, wherein the trench is provided by a two-step procedure, a first step wherein a shallow trench having a radius of curvature at corners thereof is formed, and thereafter a trench having a predetermined depth to the shallow trench is formed. Note claims 2, 5, 43 and 54.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining claims, having features as discussed previously, and further including (but not limited to) wherein the step for forming shallow trenches is carried out by isotropic etching and the step for forming trenches having a predetermined depth is carried out by anisotropic etching (see claims 3 and 6); and/or wherein providing the curvature includes forming bird's beaks at the upper end portion of the trench (note claim 12); and/or wherein providing the curvature is performed such that an angle between the circuit formation surface of the semiconductor substrate and a side surface of the semiconductor substrate forming the trench is within a range of 90° and 180° (see claim 13); and/or material of the buried insulating film and the technique for formation thereof as in claims 18-38; and/or wherein the oxidation prevention film is removed after performing the additional thermal oxidation (see, e.g., claims 39, 42, 44 and 48, as well as claims 49-53).

The invention as presently claimed in the above-identified application is directed to a method of manufacturing a semiconductor substrate, or semiconductor device, having a trench isolation structure. A process forming a so-called "trench isolation structure", which forms trenches extending into the substrate from the substrate surface and then selectively oxidizes the trenches to form a thermal oxide film, has

been employed to form insulating/isolation structure of semiconductor devices, as described in the paragraph bridging pages 1 and 2 of Applicants' specification.

In the trench isolation structure, end portions (corner points) essentially exist near the trench upper end portion of the semiconductor substrate. Stress concentration fields (both mechanical stress and electrical stress) are formed near these end portions. Because such stress concentration fields are formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape having an acute angle, as shown by the structure represented by reference character 4 in Fig. 1C of Applicants' original disclosure. If such an acute angle portion 4 remains on the semiconductor surface, however, concentration of electric field occurs at this acute angle portion during circuit operation and deteriorates the breakdown voltage characteristics of, e.g., transistors, capacitors, etc., formed using such substrate. Moreover, mechanical stress fields, which are disadvantageous, are also formed. See the paragraph bridging pages 3 and 4 of Applicants' specification.

Additional problems can arise where trenches are filled with a burying material, such as buried insulating material of chemically vapor deposited silicon oxide, for example. If additional thermal oxidation is performed after burying the buried insulating film, this additional thermal oxidation oxidizing the semiconductor substrate lining the trench, volume expansion caused by the thermal oxidation after filling the trench causes a compressing stress of the semiconductor substrate due to the volume expansion of the filled trench, such stress deteriorating characteristics of electrical devices formed using the substrate.

Against this background, Applicants provide a process wherein trench isolation can be utilized, without causing deterioration of breakdown voltage characteristics of devices such as transistors and capacitors formed using the substrate with the trench isolation structure, while providing semiconductor devices having a high reliability, and wherein compressing stresses on the semiconductor substrate lining the trench are avoided. Moreover, Applicants fabricate the structure using a relatively simple technique.

Applicants have found that the desired structure, avoiding problems as discussed in the foregoing, can be achieved by preventing a substrate shape in the proximity of the upper end portion of the device isolation trench from becoming an acute angle; and, by the present invention, provide simple techniques for preventing such acute angle, while avoiding other problems arising due to stresses in the semiconductor substrate adjacent the trenches. Specifically, according to an aspect of the present invention, Applicants provide procedures which can easily and effectively provide a curvature (increased curvature) only of an upper end portion of the trench, by an additional thermal oxidation which selectively oxidizes only the upper end portion. For example, and specifically, according to aspects of the present invention, after an initial thermal oxidation providing curvature at the upper end portion of the trench, and thereafter burying the buried insulating film, this insulating film also being formed on an oxidation prevention film on the semiconductor substrate, this insulating film on the oxidation prevention film is removed, leaving the insulating film buried in the trench; and the upper end portion of the trench is selectively thermally oxidized while lower portions of the trench (in particular, the semiconductor substrate lining the trench

extending from the upper end portion) are substantially not oxidized, whereby the semiconductor substrate can be thermally oxidized (selectively) at only the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench. Removal of the insulating film from the oxidation prevention film, prior to the additional, selective thermal oxidation, can, for example, uncover upper end portions of the trench, facilitating selective thermal oxidation of the upper end portions. Moreover, and more generally, after burying the buried insulating film and removal of this insulating film from the oxidation prevention film on the substrate, an upper end portion of the trench can be provided with curvature (increased curvature), which prevents the acute angle. Thus, prevention of the acute angle can be achieved, for example, by thermal oxidation of substantially only the upper end portion of the trench, after the initial oxidation and burying, e.g., by forming bird's beaks only at the upper end portion of the trench.

It is emphasized that according to the present, invention two thermal oxidation steps are performed with, e.g., an oxidation resistant film in place, a first prior to burying the trench and a second after burying the trench, the second thermal oxidation being performed as a selective thermal oxidation that oxidizes only upper end portions of the trench. With the two thermal oxidations, particularly wherein the second (additional) thermal oxidation thermally oxidizing only upper end portions of the trenches, the aforementioned acute angle can be avoided, while also avoiding undesirable compressing stresses on the semiconductor substrate lining the trenches.

Thus, according to the present invention as claimed in the above-identified application, there are two thermal oxidation steps, with the trench being buried between

the first and second thermal oxidation steps. In the first thermal oxidation step, an oxidation film is formed on the surface of the trench, with a curvature to some degree being formed at the upper end of the trench. Since this first thermal oxidation film is formed before the trench is buried, even by carrying out thermal oxidation with volume expansion by oxidizing the trench, since the trench is not filled a compressing stress does not form along the substrate lining the trench, so that deterioration of electrical properties, due to such compressing stress, is avoided.

In the second thermal oxidation step, the additional thermal oxidation is carried out in the condition that an insulating film is buried in the trench; accordingly, only the upper end portions of the trench are selectively thermally oxidized, without thermally oxidizing other portions of the semiconductor substrate lining the trench. Thus, since, e.g., bottom portions and bottom side portions of the trench are not thermally oxidized, deterioration of the properties due to compressing stress can be avoided. Furthermore, since upper end portions of the trench are selectively thermally oxidized, a sufficient curvature is formed at upper end portions of the trench, avoiding the sharp angle thereat and adverse effects thereof.

According to various aspects of the present invention, including selective oxidation of only upper end portions of the trench in the additional oxidation step, various advantages are achieved, including avoidance of an increase of stress due to compressing stress along the substrate lining the trench, and narrowing of the element formation region due to enlargement of bird's beak at the upper end portions of the trench. In other words, according to the present invention, sufficient curvature is achieved to avoid decrease in electrical properties caused by the sharp angle at the

upper end portions of the trench, while disadvantageous narrowing of the element formation region due to undue enlargement of the bird's beak at the upper end portions of the trench can be avoided.

Applicants' original disclosure clearly sets forth advantages according to the present invention, having the two thermal oxidation steps, the oxidation resistant film formation, and etching back the burying insulating film. That is, as is clear according to the specification of the above-identified application, since the buried insulating film 9 (see, e.g., Fig. 6G and 6H of Applicants' original disclosure) has already been formed inside the trench of the silicon substrate 1, especially wherein the insulating film 9 has been removed from on the oxidation prevention film (e.g., at the upper end portion of the trench), oxidation proceeds from near the trench upper end portion 12, as the inside of the trench is hardly oxidized. That is, a longer time is necessary for oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 at lower portions of the trench, than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially near the bottom of the trench.

On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench side walls and the upper surface of the trench exists at the trench upper end portion 12, and oxidation seeds can diffuse at a relatively high rate along this weak boundary layer, and especially where the insulating film has been removed from on the oxidation prevention film. As a result, oxidation seeds are supplied to the trench upper end portion 12 within a short time, so that only the portions in the proximity of the trench upper end portion 12 are oxidized

preferentially and the formation of the radius of curvature at the trench upper end portion 12 is promoted.

Note, for example, the paragraph bridging pages 24 and 25 of Applicants' specification, referring, inter alia, to the first embodiment. See also the paragraph bridging pages 14 and 15 of Applicants' specification, in connection with the first embodiment. See also page 26 of Applicants' specification, in connection with the third embodiment.

Mehta, et al. discloses a fabrication method for creating wide and narrow isolation regions. The method includes steps of selectively providing an etch resist layer over the wide spacing and exclusive of the narrow spacing, etching the semiconductor structure to increase the depth of the narrow spacing to form a narrow trench, growing an oxide liner in the narrow trench and in the wide spacing, providing a trench fill oxide layer over the nitride layer and the oxide liner in the wide spacing and in the narrow trench, and field oxidizing the wide spacing and the narrow trench. See column 2, lines 4-12. Note also column 2, lines 22-32 and 51-53. Note further column 3, lines 5-7. In a specific embodiment shown in Figs. 5 and 6, this patent discloses that after layer 60 is subjected to an oxide etch, structure 12 is subjected to thermal oxidation to grow the oxide in spacing 44 and 46 by local oxidation of silicon techniques. The growing of layers 60 in spacings 44 and 46 provides a deeper insulative region in both regions 24 and 28 of structure 12. Once subjected to thermal oxidation, the insulative material in regions 24 and 28 grows in a direction toward nitride layer 18 and base 14; and, therefore, providing conventional LOCOS operation

on spacings 44 and 46 creates effective isolation regions 24 and 28 for structure 12. See column 5, lines 55-65.

It is emphasized that according to the teachings of Mehta, et al., in the thermal oxidation after layer 60 has been subjected to oxide etch, layers 60 grows providing a deeper insulative region in both regions 24 and 28, the insulative material in regions 24 and 28 growing, inter alia, in a direction toward base 14. It is respectfully submitted that this disclosure in Mehta, et al., with respect to growth of the thermal oxide towards the base 14, would have neither disclosed nor would have suggested, and in fact would have taught away from, the presently claimed invention, including wherein the selective thermal oxidation is performed to oxidize only a portion of the substrate at the upper end portion of the trench, and not substantially at other portions of the substrate lining the trench, to provide an increase in curvature of the upper end portion of the trench substantially without oxidizing other portions of the semiconductor substrate lining the trench.

It is respectfully submitted that Mehta, et al. has an entirely different purpose from that of the present invention. That is, Mehta, et al. is concerned with providing a narrow trench isolation region and a wide LOCOS isolation region, for eliminating or reducing dishing due to different widths of trench isolation regions. In contrast, the present invention is directed to avoiding deterioration of electrical properties due to sharp angles and/or stresses arising with trench isolation. Particularly noting the purpose of Mehta, et al., including the purpose of growing the insulative material in a direction toward the base, as described in column 5, lines 55-65, this patent would have taught away from the present invention.

The contention by the Examiner that Mehta, et al. discloses performing oxidation so as to oxidize only a portion of the semiconductor substrate at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, is respectfully traversed. Again, it is emphasized that Mehta, et al. specifically discloses thermal oxidation to grow the insulative material in regions 24 and 28 in a direction towards base 14, and provides a deeper insulative region. Such disclosure would have taught away from, and clearly would have neither disclosed nor would have suggested, performing oxidation so as to oxidize only a portion of the substrate at the upper end portion of the trench, as in the present invention.

During the above-mentioned interview, the Examiner pointed to Mehta, et al. as having shallow and deep trenches, not a field oxide formed by local oxidation of silicon of the substrate. However, while Mehta, et al. discloses wide and narrow trenches, clearly this patent discloses relatively long thermal oxidation after forming the burying material, growing the oxide in spacings 44 and 46 by local oxidation of silicon, providing a deeper insulative region in both regions 24 and 28 of structure 12. Clearly this disclosure, providing a deeper insulative region, describes thermal oxidation at other portions of the semiconductor substrate lining the trench, other than at the upper end portion of the trench; and, as indicated previously, would have taught away from the present invention.

It is respectfully submitted that the additional teachings of Otsu would not have rectified the deficiencies of Mehta, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Otsu discloses a method of fabricating a metal -insulator-semiconductor device in which a gate electrode is formed to cover the upper portion of a device forming region which is isolated by a trench, including a step of forming a laminated film including at least an oxidation proof film on a substrate, selectively moving parts of the laminated film and a part of the substrate beneath the laminated film to thereby form the trench in the substrate, burying an insulation film in the trench, and performing a selective oxidation on an entire surface of the insulation film. See column 2, lines 43-55. Note also the paragraph bridging columns 2 and 3, which describes that selective oxidation is carried out after an insulation film is buried in the trench, so that the edge portions of element or device forming regions of the substrate can be formed to be round; and after formation of a gate insulation film, the thickness of the gate insulation film at the edge portions of the device forming region can be made sufficiently large. See also column 4, lines 3-7, 39-47 and 52-58. Note also column 5, lines 5-16.

Initially, it is respectfully submitted that the teachings of Otsu are not properly combinable with the teachings of Mehta, et al. That is, Otsu, as applied by the Examiner, is directed to a selective oxidation. On the other hand, Mehta, et al. has a purpose of extending the layers 60 to provide a deeper insulative region in both regions 24 and 28 of structure 12. It is respectfully submitted that by combining the teachings of Mehta, et al. and Otsu as applied by the Examiner, such combination would destroy Mehta, et al. for its intended purpose of providing a deeper insulative region. Accordingly, one of ordinary skill in the art would not have combined the teachings of Mehta, et al. and Otsu as applied by the Examiner. See In re Ratti, 123 USPQ 359 (CCPA 1959).

In any event, even assuming, arguendo, that the teachings of Mehta, et al. and Otsu were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed method, including the two thermal oxidation steps and trench filling step therebetween, particularly in the presence of the oxidation resistant film, and decreased acute angle at upper end portions of the trench while avoiding compressing stresses in the semiconductor substrate lining the trenches, and advantages achieved thereby, as discussed in the foregoing.

It is respectfully submitted that the additional teachings of Yuzuriha would not have rectified the deficiencies of the combined teachings of Mehta, et al. and of Otsu, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Yuzuriha discloses a semiconductor device in which an oxide film is easily buried in a trench and a trench for applying small leakage current is formed. The semiconductor device is formed by isotropically plasma-etching a silicon substrate with an oxide film as a mask, whereby forming a recess of circular-arc-shaped section, with the recess being anisotropically etched with the oxide film 2 as a mask to provide a trench 3 of desired depth, thereby forming a trench having a taper in the opening.

Even assuming, arguendo, that the teachings of Yuzuriha were properly combinable with the teachings of Mehta, et al., or of Otsu, as indicated previously it is respectfully submitted that the teachings of Mehta, et al. and Otsu would not have been properly combinable, such that the teachings of the references as applied in Item 5 on page 12 of the Office Action mailed July 3, 2003 would have neither disclosed nor

would have suggested the presently claimed invention, including the thermal oxidation steps and filling of the trench, e.g., in the presence of the oxidation resistant film. Even assuming, arguendo, the teachings of each of Mehta, et al., Otsu and Yuzuriha were properly combinable, such combined teachings would have neither disclosed nor would have suggested the two thermal oxidation steps, sandwiching formation of the buried insulating material, and advantages thereof as discussed previously.

With respect to the subject matter of claims 4, 24-26, 45, 50 and 53, it is respectfully submitted that the combined teachings of Mehta and Otsu would have neither disclosed nor would have suggested the presently claimed subject matter.

Mehta discloses trench isolation and local oxidation of silicon (LOCOS) isolation processes, which include steps of forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the semiconductor substrate; filing the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. Note particularly the paragraph bridging columns 3 and 4 of this patent. Note also column 4, lines 47-51; column 5, lines 37-42 and 64-67; and column 6, lines 4-9 and 18-22.

Mehta discloses a method including wherein a second thermal oxidation is to form a LOCOS field oxide. It is respectfully submitted that such forming of the LOCOS field oxide, requiring a relatively long thermal oxidation, would have neither taught nor would have suggested, and in fact would have taught away from, the selective thermal

oxidation of the semiconductor substrate so as to oxidize only a portion of the semiconductor substrate at the upper end portion of the trenches and not substantially at other portions of the semiconductor substrate lining the trenches, the upper end portion not covered by the oxidation prevention film being oxidized, so as to increase a curvature of the upper end portions of the trenches, substantially without oxidizing the other portions of the semiconductor substrate lining the trenches, as in claim 4; and the corresponding recitations in step (f) of claim 45.

The contention by the Examiner that Mehta discloses performing oxidation of the semiconductor substrate so as to oxidize only a portion of the semiconductor substrate at the upper end portion of the trenches, and not substantially at other portions of the semiconductor substrate lining the trenches, set forth on page 16 of the Office Action mailed July 3, 2003, is respectfully traversed. It is noted that the Examiner has pointed to no portion of Mehta as describing such oxidation of only a portion of the semiconductor substrate at the upper end portion of the trenches. Particularly in light of the reasoning set forth in the foregoing, wherein the LOCOS field oxide formation would require relatively long thermal oxidation, it is respectfully submitted that Mehta would have taught away from the present invention including the oxidation of only a portion of the substrate at the upper end portion of the trenches, and other recitations of the present claims as discussed previously.

It is respectfully submitted that the teachings of Otsu would not have rectified the deficiencies of Mehta, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

The teachings of Otsu have been previously discussed. As with Mehta, et al., it is respectfully submitted that the teachings of Otsu and Mehta, as applied by the Examiner, would destroy Mehta for its intended function of providing the LOCOS field oxide; in view thereof, it is respectfully submitted that one of ordinary skill in the art involved with in Mehta, would not have looked to the teachings of Otsu. See In re Ratti, supra.

In any event, even assuming, arguendo, that the teachings of Mehta and of Otsu were properly combinable, such combined teachings would have neither disclosed nor would have suggested the combination of steps as in the present claims, including the two thermal oxidations, burying the buried insulating film and forming of the oxidation prevention film, and advantages achieved by the present invention due to the processing steps of the present claims.

It is respectfully submitted that the combined teachings of Mehta and Yuzuriha would have neither disclosed nor would have suggested the subject matter of claims 54 and 55, including, inter alia, the thermal oxidation steps and burying of the buried insulation film; and in particular the additional thermal oxidation being performed so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench, to increase the radius of the curvature in the proximity of the upper end portion of the trench, and substantially without oxidizing other portions of the semiconductor substrate lining the trench, especially with the formation of the trench being performed by first and second trench-forming steps respectively using isotropic and anisotropic etching, and advantages achieved due thereto. Again emphasizing that Mehta discloses forming a LOCOS field oxide which would require relatively long periods of

thermal oxidation, the disclosure of this patent would have taught away from the presently claimed method including wherein the additional thermal oxidation is performed to selectively oxidize the substrate at the upper end portion of the trench, substantially without oxidizing other portions of the semiconductor substrate lining the trench, as in claim 54.

In view of the foregoing comments and amendments to the claims, granting of the concurrently filed Request for Continued Examination and entry of the present amendments, and reconsideration and allowance of all claims remaining in the application, are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (500.36904X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

William I. Solomon

William I. Solomon
Registration No. 28,565

1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209
Tel.: 703-312-6600
Fax.: 703-312-6666
WIS/sjg